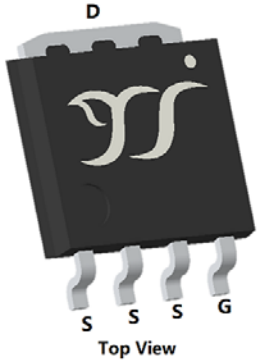
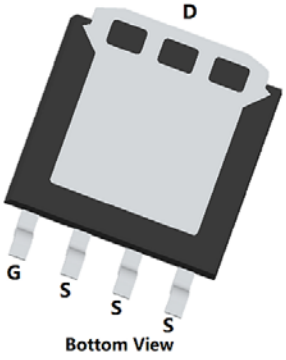
N-Channel Enhancement Mode Field Effect Transistor

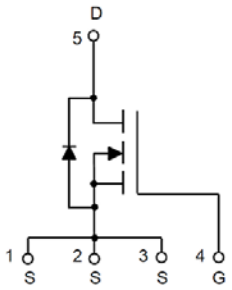


Top View



Bottom View

LFPAK56



Product Summary

- V_{DS} 40V
- I_D 225A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜1.4mΩ
- 100% EAS Tested
- 100% ▽V_{DS} Tested
- ESD Level(HBM) H1C

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free
- Part no. with suffix “Q” means AEC-Q101 qualified

Applications

- EPS
- 12V BMS
- High-power motor

■ Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V_{DS}	-	40	V
Gate-source Voltage			V_{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25℃,V_{GS}=10V	I_D	-	32.5	A
		T_A=100℃,V_{GS}=10V		-	23	
Continuous Drain Current (Note 1,3)	Steady-State	T_C=25℃,V_{GS}=10V,Chip limitation		-	225	
		T_C=100℃,V_{GS}=10V		-	159	
Pulsed Drain Current	T_C=25℃,t_p≤10μs		I_{DM}	-	900	
Maximum Body-Diode Continuous Current	T_C=25℃		I_S		109	
Avalanche energy (non-repetitive)	T_J=25℃,V_G=10V, R_G=25Ω, L=0.5mH, I_{AS}=47A		EAS	-	552.2	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25℃	P_D	-	2.7	W
		T_A=100℃		-	1.35	
Total Power Dissipation (Note 1,3)	Steady-State	T_C=25℃		-	130	
		T_C=100℃		-	65	
Junction and Storage Temperature Range			T_J ,T_{STG}	-55	175	℃

■Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	55.4	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	1.15	

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=1mA,Tj=25℃	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V,V_{GS}=0V,Tj=25℃	-	-	1	μA
		V_{DS}=40V,V_{GS}=0V,Tj=125℃	-	-	100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V,Tj=25℃	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA,Tj=25℃	2	3	4	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V,I_D=50A,Tj=25℃	-	1.1	1.4	mΩ
Diode Forward Voltage	V_{SD}	I_S=50A,V_{GS}=0V,Tj=25℃	-	0.82	1.2	V
Gate Resistance	R_G	f=1MHz,Tj=25℃	-	0.85	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=20V,V_{GS}=0V,f=1MHz,Tj=25℃	-	4607	-	pF
Output Capacitance	C_{oss}		-	1394	-	
Reverse Transfer Capacitance	C_{rss}		-	84	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=20V,I_D=50A,Tj=25℃	-	63	-	nC
Gate-Source Charge	Q_{gs}		-	19	-	
Gate-Drain Charge	Q_{gd}		-	11	-	
Reverse Recovery Charge	Q_{rr}	I_F=50A,di/dt=100A/μs,V_{GS}=0V,V_R=20V, Tj=25℃	-	24	-	nC
Reverse Recovery Time	t_{rr}		-	37	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DS}=20V,I_D=50A,R_{GEN}=3Ω, Tj=25℃	-	21.4	-	ns
Turn-on Rise Time	t_r		-	135	-	
Turn-off Delay Time	$t_{D(off)}$		-	39	-	
Turn-off Fall Time	t_f		-	16.4	-	

Note：

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with T_A=25℃.The maximum allowed junction temperature of 175℃. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).

■Typical Electrical and Thermal Characteristics Diagrams

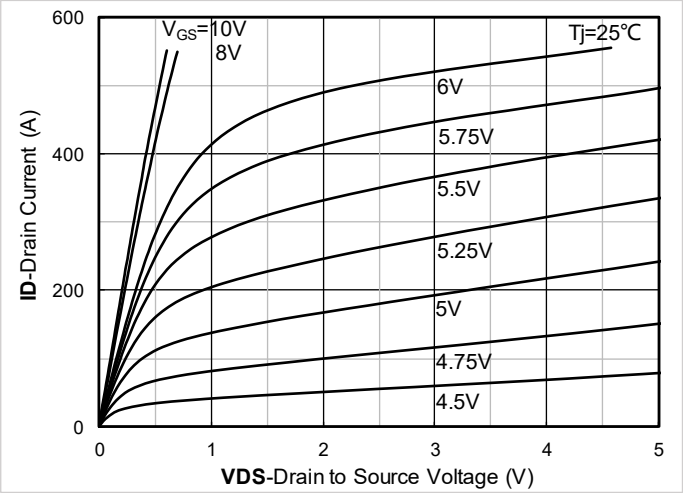


Figure 1. Output Characteristics; typical values

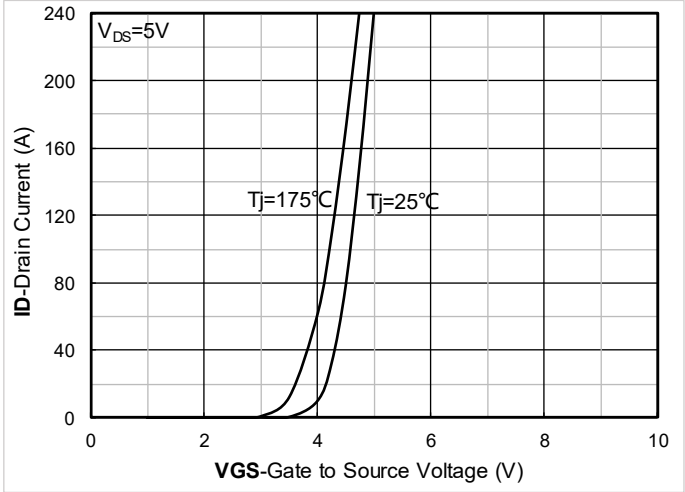


Figure 2. Transfer Characteristics; typical values

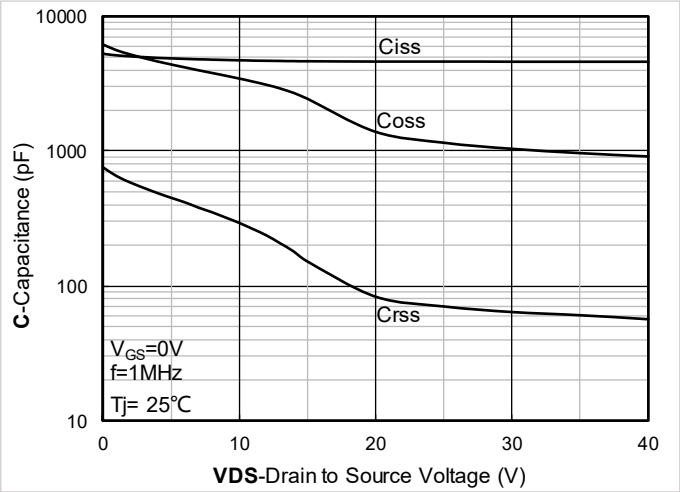


Figure 3. Capacitance Characteristics; typical values

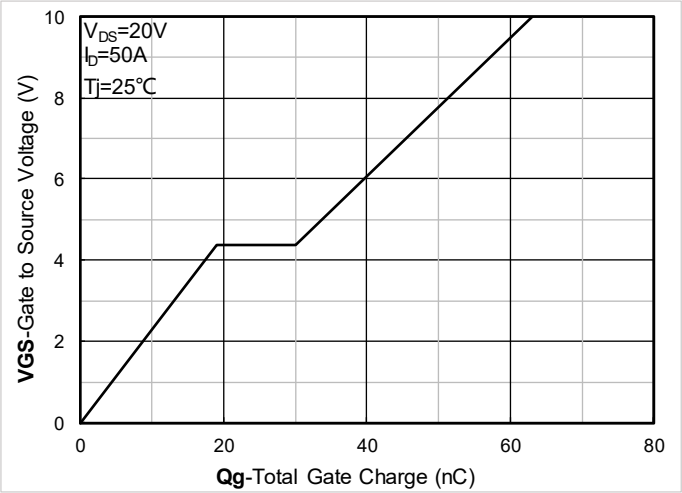


Figure 4. Gate Charge; typical values

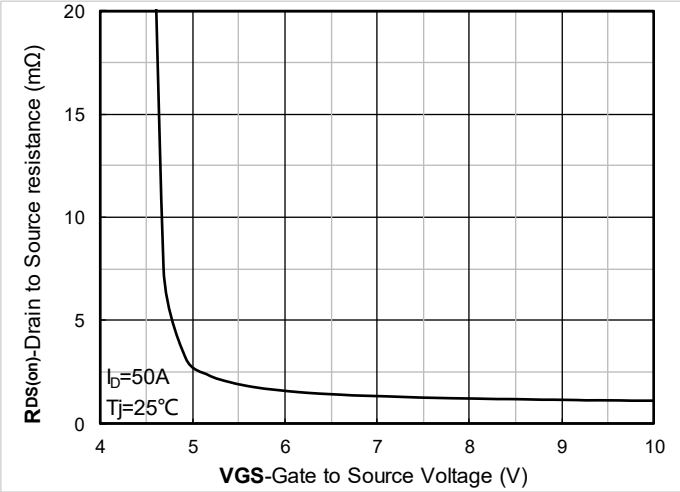


Figure 5. On-Resistance vs Gate to Source Voltage; typical values

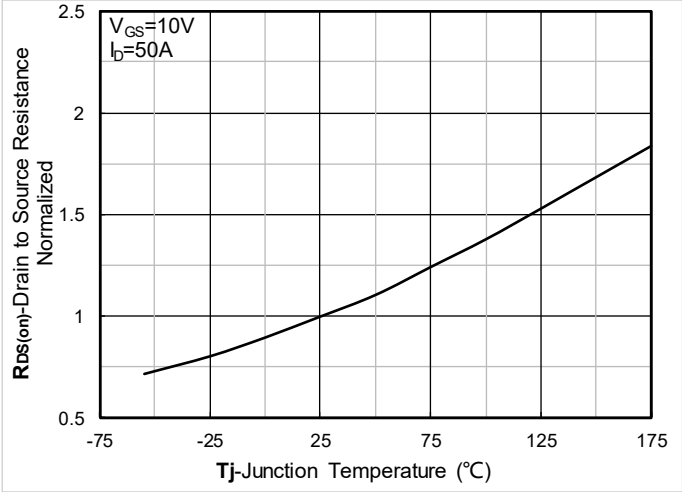


Figure 6. Normalized On-Resistance

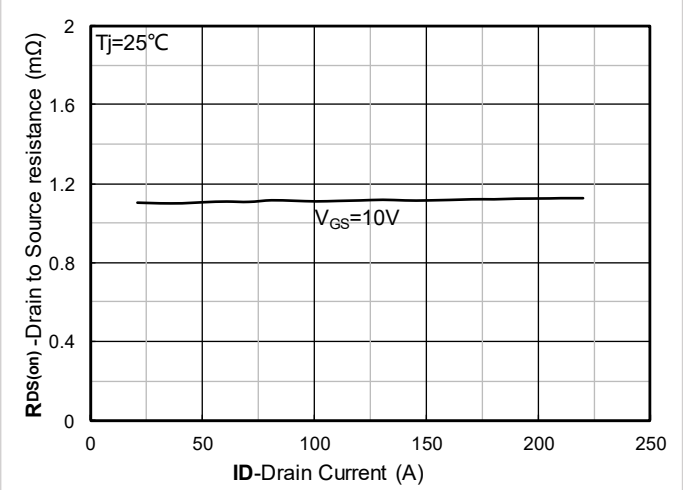


Figure 7. $R_{DS(on)}$ VS Drain Current; typical values

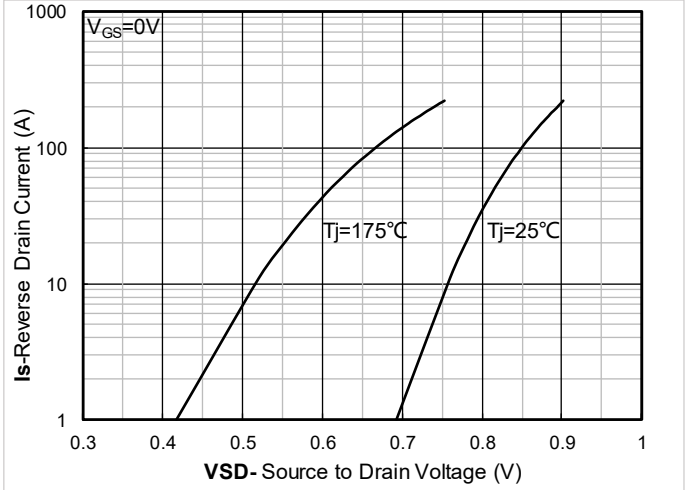


Figure 8. Forward characteristics of reverse diode; typical values

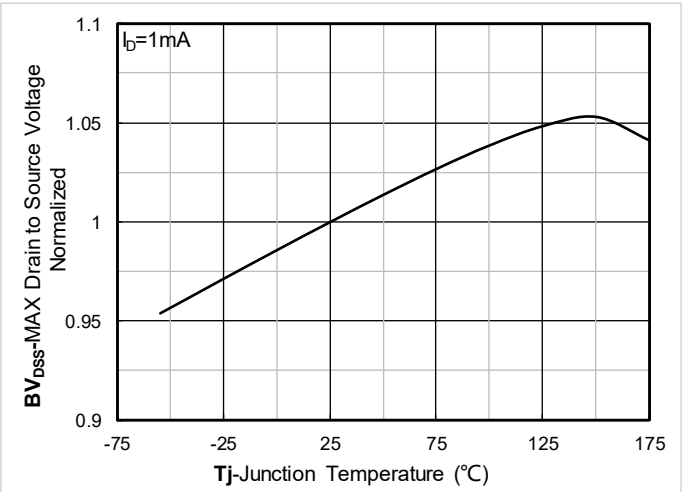


Figure 9. Normalized breakdown voltage

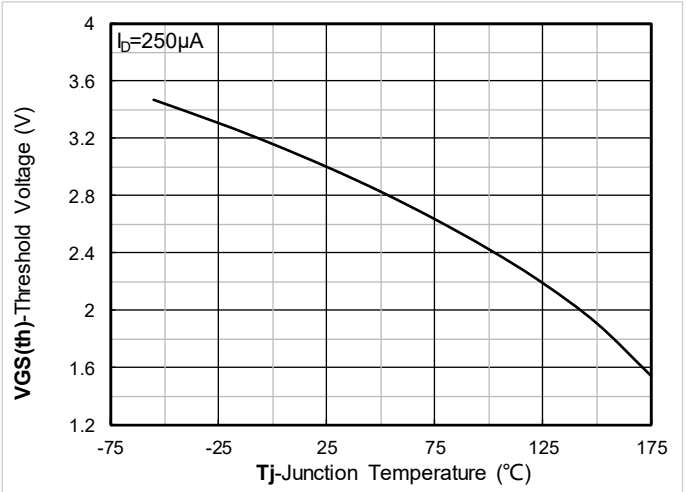


Figure 10. Gate Threshold voltage; typical values

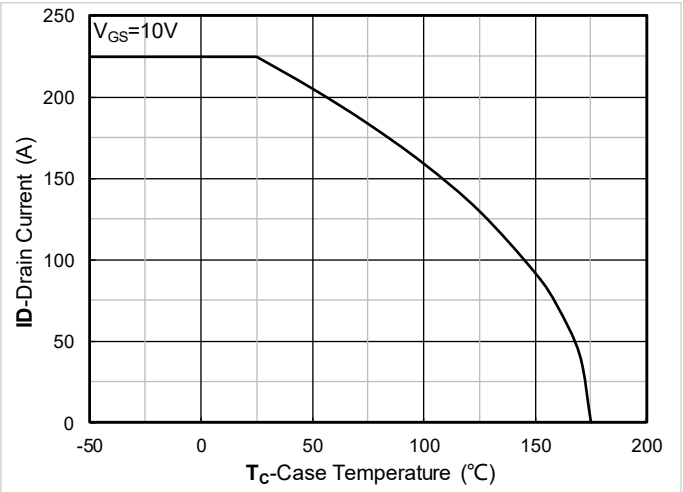


Figure 11. Current dissipation

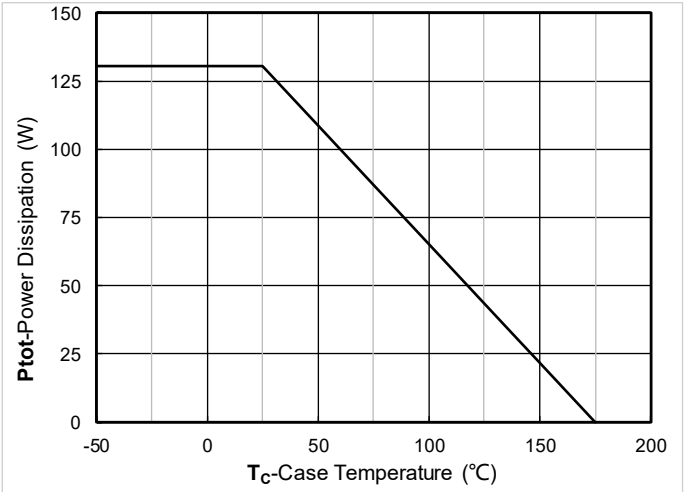


Figure 12. Power dissipation

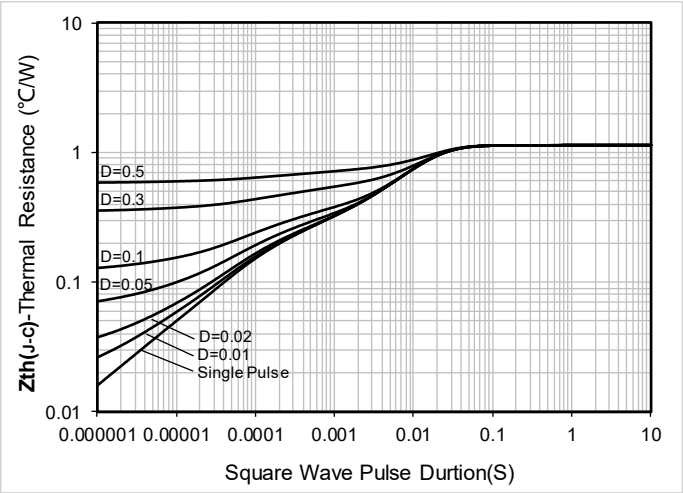


Figure 13. Maximum Transient Thermal Impedance

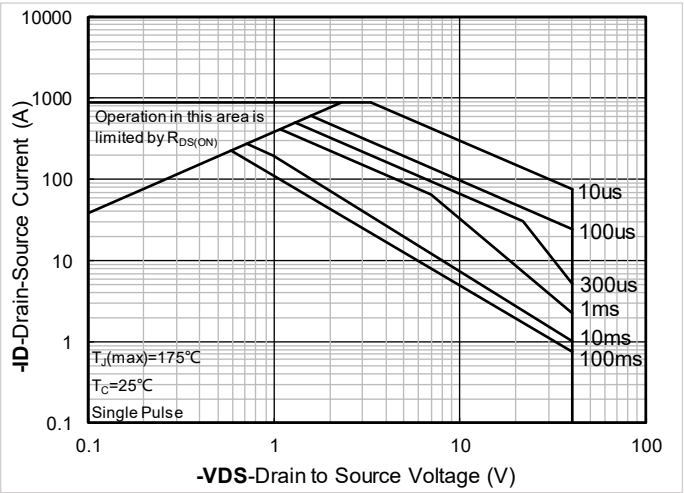


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

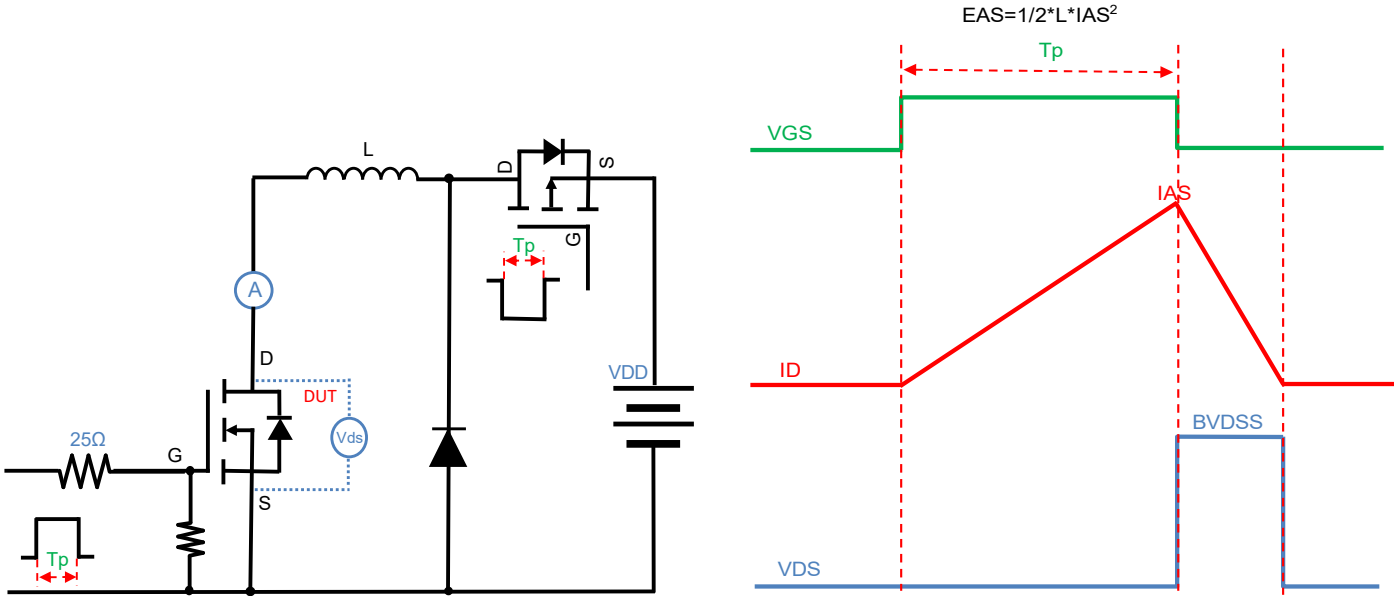


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

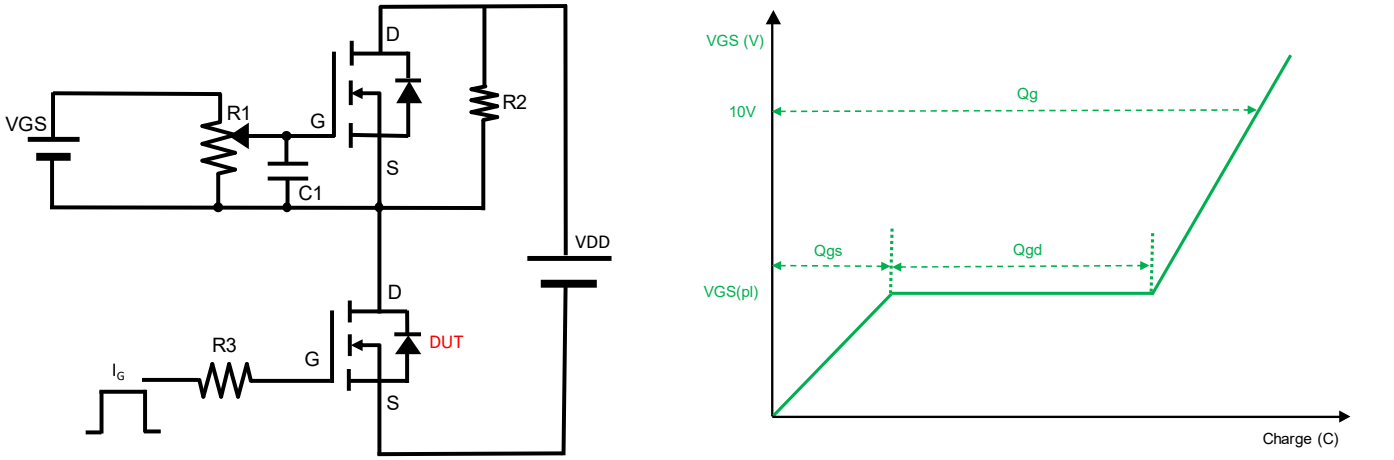


Figure B. Gate Charge Test Circuit & Waveform

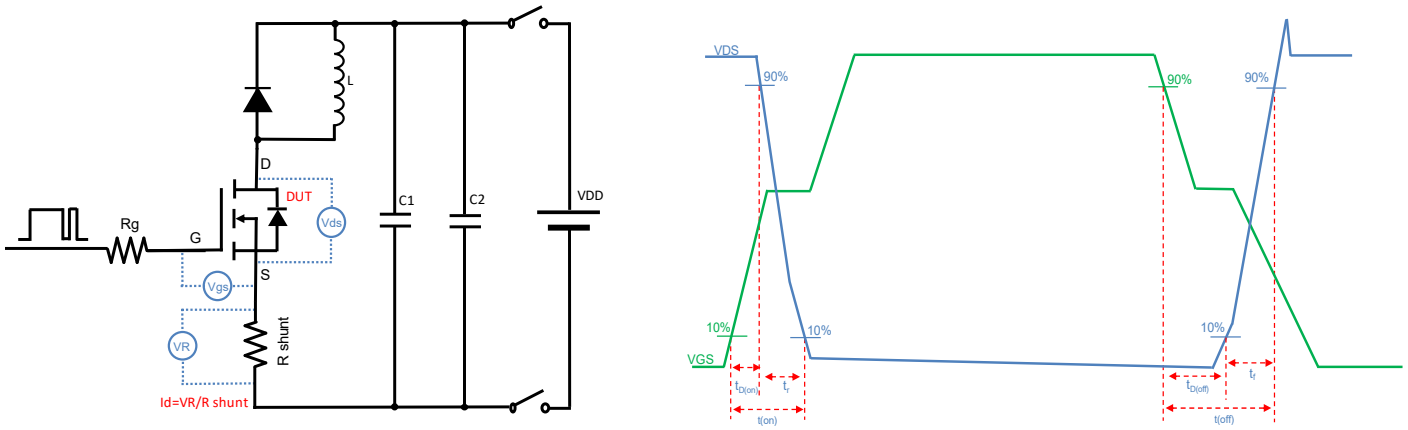


Figure C. Resistive Switching Test Circuit & Waveform

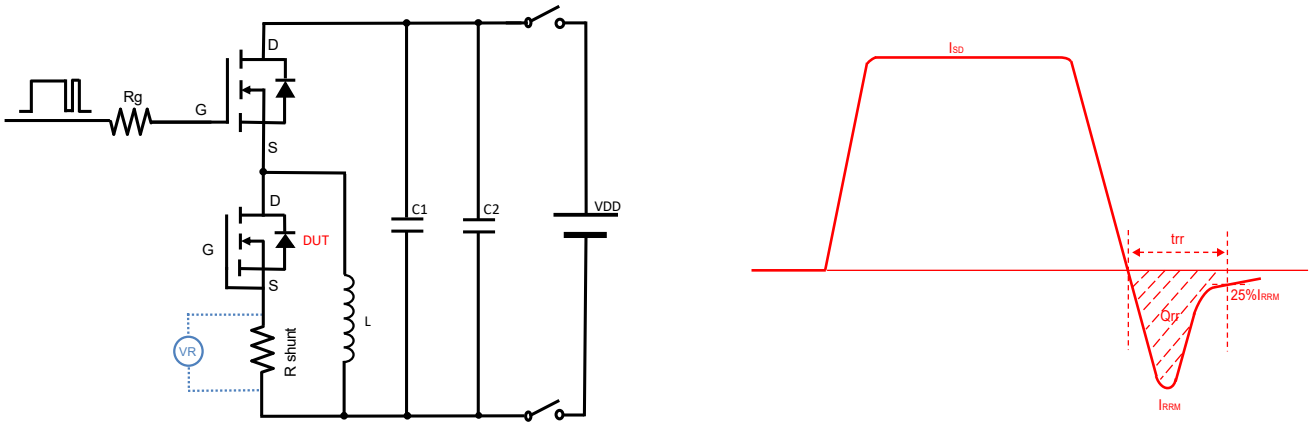
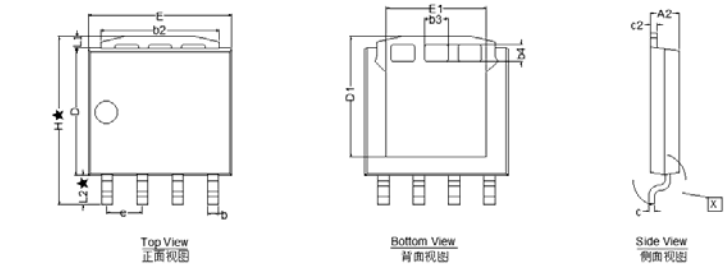
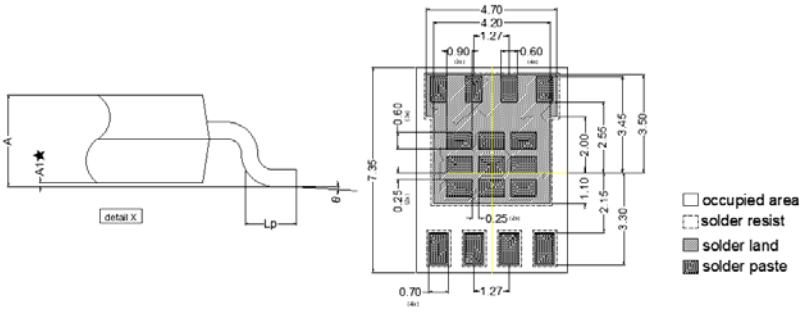


Figure D. Diode Recovery Test Circuit & Waveform

■ LFPAK56E-8L-A-1.04MM Package information



SYMBOY	MILLIMETER		
	MIN	NOM	MAX
A	1.01	1.11	1.2
A1	0.00	0.05	0.10
A2	0.95	1.04	1.10
b	0.35	0.42	0.5
b2	4.11	4.26	4.41
b3	0.75	0.85	0.95
b4	0.5	0.6	0.70
c	0.19	0.22	0.25
c2	0.24	0.27	0.3
D	4.45	4.6	4.70
D1	4.25	4.35	4.45
E	4.95	5.15	5.30
E1	3.50	3.6	3.70
e		1.27	
H	5.90	6.05	6.20
Lp	0.40	0.63	0.85
L1	0.30	0.4	0.50
L2	0.90	1.05	1.30
θ	0°		8°

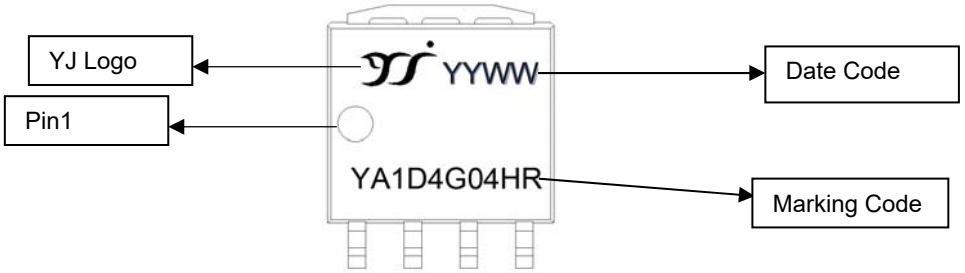


Recommended stencil thickness: 0.125mm

Note:

1. All dimensions are in millimeters (mm) unless otherwise specified.
［所有尺寸均以毫米为单位，除非另有说明］
2. General tolerances: ±0.10mm unless otherwise specified.
［通用公差为±0.10mm，除非另有说明］
3. Dimensions and tolerances per ASME Y14.5M-2018.
［尺寸和公差遵循 ASME Y14.5M-2018 标准］
4. All dimensions shown are exclusive of burrs and gate residues. Burrs and gate vestiges shall not exceed 0.15 mm in maximum.
［所有尺寸均不包括毛刺和浇口残留。毛刺与浇口残留的尺寸最大不得超过 0.15mm］
5. Dimension b does not include dambar protrusion of max 0.100 mm per side.
［尺寸b不包括单边最大0.100 MM的中筋凸出部分］
6. Dimensions D and E are the overall extreme outer dimensions of the mold compound. These dimensions exclude mold flash, lead flash, protrusions and burrs but include the maximum allowable mold mismatch.
［D和E是塑封体的外部极限尺寸，不包括包封溢料、内引线溢料、凸出部分以及胶体毛刺，但是包含了包封错位的最大尺寸］
7. Formed leads shall be planar with respect to one another within a maximum of 0.076 mm relative to the seating plane.
［成型的管脚应为同一平面，共面性最大为0.1mm］
8. ★It is the key size.
［★ 标记为关键尺寸］

■ Marking Information



Note：
1. All marking is at middle of the product body
2. All marking is in laser printing
3. YA1D4G04HR is marking code, YYWW is date code, “YY” is year, “WW” is week
4. Body color: Black

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